

CLAIMS

What is claimed is:

- 1 *sub 7* 1. An integrated circuit comprising:
2 *A4* a test controller;
3 *e* at least one logic unit controller; *deskew*
4 *b* a test bus coupled between the test controller and the
5 at least one logic unit controller;
6 *c* at least one design for test feature coupled to the at
7 least one logic unit controller; and
8 *d* *Testers* a logic unit coupled to the at least one design for test
9 feature.

1 2. The integrated circuit of claim 1 wherein the test
2 controller is an integrated test controller

1 3. The integrated circuit of claim 1 wherein the logic
2 unit controller is a deskew controller

1 4. The integrated circuit of claim 1 wherein the test
2 bus is an internal test bus.

1 5. The integrated circuit of claim 4 wherein the
2 internal test bus includes n number of lines such that

$$n = a + \log_2 i$$

4 where n = number of lines, a = number of ancillary
5 transmission bits, and $\log_2 i$ = number of instruction bits.

1 6. The integrated circuit of claim 5 wherein the number
2 of instruction bits are represented within the content of an

instruction register that is compliant with IEEE 1149.1.

7. The integrated circuit of claim 5 wherein the ancillary transmission bits include at least one of a clock signal, at least one state of a test access port finite state machine, a security bit, a test data input, and a counter value.

8. The integrated circuit of claim 7 wherein the at least one state of a test access port finite state machine are encoded into three bits.

9. The integrated circuit of claim 7 wherein the at least one state of a test access port finite state machine is allocated into a one-bit test-logic-reset state, a one bit run-test/idle state, and a two-bit residual state.

10. A platform comprising:
an external device;
a support structure;
a controller disposed on the support structure and coupled to the input device;
at least one memory chip disposed on the support structure and coupled to the controller through a processor bus; and
an integrated circuit having a test controller, at least one logic unit controller, a test bus coupled between the test controller and the at least one logic unit controller, at least one design for test feature coupled to the logic unit controller, and a logic unit coupled to the at least one

14 design for test feature.

1 11. The platform of claim 10 wherein the external device
2 is at least one of a keyboard, a mouse, and a modem.

1 12. The platform of claim 10 wherein at least one of the
2 following is true: the test controller is an integrated test
3 controller; the logic unit controller is a deskew controller;
4 and the test bus is an internal test bus.

1 13. The platform of claim 12 wherein the internal test
2 bus includes n number of lines such that

3
$$n = a + \log_2 i$$

4 where n = number of lines, a = number of ancillary
5 transmission bits, and $\log_2 i$ = number of instruction bits.

1 14. The platform of claim 13 wherein the number of
2 instruction bits are represented within the content of an
3 instruction register that is compliant with IEEE 1149.1.

1 15. The platform of claim 13 wherein the ancillary
2 transmission bits include at least one of a clock signal, at
3 least one state of a test access port finite state machine, a
4 security bit, a test data input, and a counter value.

1 16. The platform of claim 15 wherein the at least one
2 state of a test access port finite state machine are encoded
3 into three bits.

1 17. The platform of claim 15 wherein the at least one
2 state of a test access port finite state machine is allocated

3 into a one bit test-logic-reset state, a one bit run-
4 test/idle state, and a two bit residual state.

1 18. A method comprising:

2 generating a test information packet in a test
3 controller of an integrated circuit;

4 transmitting the test information packet to at least one
5 logic unit controller over a test bus coupled between the
6 test controller and the at least one logic unit controller;

7 processing the test information packet within the at
8 least one logic unit controller to generate at least one test
9 control signal; and

10 transmitting the at least one test control signal to the
11 at least one design for test feature coupled to the logic
12 unit controller.

1 19. The method of claim 18 further comprising:

2 interacting with a logic unit coupled to the at least
3 one design for test feature based on the at least one test
4 control signal.

1 20. The method of claim 19 wherein transmitting the test
2 information packet to at least one logic unit controller over
3 the test bus includes transmitting the test information
4 packet over n number of lines such that

5
$$n = a + \log_2 i$$

6 where n = number of lines, a = number of ancillary
7 transmission bits, and $\log_2 i$ = number of instruction bits.